PATENT ABSTRACTS OF JAPAN

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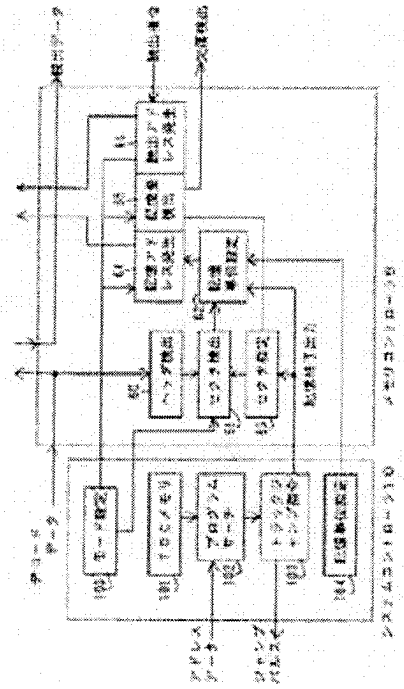
(54) HIGH SPEED REPRODUCING CIRCUIT

(57)Abstract:

PURPOSE: To realize high speed reproduction without the delay of response in a mini disk player.

CONSTITUTION: The number of sound groups to be reproduced and stored continuously is set in a storage unit specifying means 104 as a specified value previously and the specified value is stored in a storage unit setting circuit 62 at the time of setting a high speed reproducing mode. Decode data is inputted to a sector detection circuit 61 through a header detection circuit 60 and storage timing is detected, and the storage instruction by period suitable for the specified value is generated from the storage unit setting circuit 62 synchronizing with the timing and a storage address is generated from a storage address generation circuit 64 and the decode data by a prescribed number of sound groups is stored in a memory. Then the decode data is read from the memory in sound group successively from a read address generation circuit 66 by read instruction issued from an ATRAC decoder.



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1]Choose a fixed quantity of reproduction compression audio data which carries out the track jump of the spiral shape recording track which recorded voice data which carried out the data compression, and is obtained by carrying out ** intermittent reproduction, and it memorizes one by one in a memory, In a minidisc player which carries out data decompression processing of the data read one by one, and forms a fast reproduction audio signal from said memory, A fast reproduction circuit providing a storage-unit setting circuit which specifies reproduction compression audio data volume which carries out a selective memory so that memorized data in said memory may be mostly read by the next memory start during high speed reproduction mode set time.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to the fast reproduction circuit of a minidisc player.
[0002]
[Description of the Prior Art]It is attached to the MD recorder which made audio record reproduction possible, and the 160-168th page of the December 9, 1991 item of the magazine "Nikkei electronics" of the Nikkei McGraw-Hill, Inc. issue succeeds in description. This MD recorder carries out the data compression of about 1/of the sounds for two channels to 5, carries out [sound / for about 2 seconds] intermittent recording as information for about 0.5 second, and forms a recording track, A sound is reproduced by memorizing in a memory and carrying out elongation processing of the read data for the memorized information to it continuously, reproducing this recording track one by one at the time of reproduction. The data configuration of one cluster of each intermittent recording track, The whole comprises 36 sectors and compression audio data is arranged as main data by 32 sectors in which indicative datas, such as words of karaoke, follow one sector which the fixed data no information is [fixed data] in three sectors to precede follow as link data as sub data.
[0003]The address information called a header is provided in the head part of each sector, and the cluster number and the sector number are added to this address information. Therefore, sub data can detect and identify this sector number. The main data of two sectors contains 11 sound groups.
In reproduction, a unit succeeds these two sectors in intermittent reproduction.
As a result, it is constituted so that the maximum regenerative data may be memorized by the memory at the time of ordinary reproduction.

[0004]Drawing 2 is a circuit block figure of the reproduction portions of this MD recorder. The optical pickup 1 which plays the recording track of a disk optically has inputted into the servo circuit 13, the address decoder 3, and the EFM decoder 4 the output which inputted the reproducing output into RF amplifier 2, and amplified it. From a reproduction amplified output, said servo circuit 13 forms a tracking control signal and a focus control signal, and supplies them to said optical pickup 1 and the feed motor 12, and. The roll control signal formed based on the synchronized signal obtained via the system controller 10 is formed, and the disk motor 11 is supplied. Therefore, a disk is maintained at a constant linear velocity by said disk motor 11, and said pickup 1 follows in footsteps of a recording track correctly, and it coincides the focus with a recording track side.
[0005]Said address decoder 3 detected the ADIP code produced by carrying out FM recovery of the high-frequency component of the inner tracking error signal of a reproduction amplified output, and has inputted it into the EFM decoder 4. This FM decoder 4 chooses the sub-code detected within the EFM decoder 4, or the ADIP code inputted according to the selection signal acquired from said system controller 10, and supplies it to said system controller 10. Said EFM decoder 4 has also separated the synchronized signal with the sub-code.
The synchronized signal is supplied to the system controller 10.
Said system controller 10 supplies a synchronized signal to the servo circuit 13, and performs access control of a pickup based on the sub-code or the ADIP code which shows a playback position, and enables intermittent reproduction by interlaced scanning.
[0006]An error correction etc. are processed in the CIRC decoder 5, and the data by which the EFM recovery was carried out is inputted into the memory controller 6. This memory controller 6 carries out update storage of two every sectors of the decoding data repeatedly inputted by jump reproduction of the optical pickup 1, and make said memory 7 memorize it, and. The data memorized by said memory 7 according to the reading command of the latter ATRAC decoder 8 is read one by one per sound group. Said memory controller 6 is making the maximum decoding data always memorize to the memory 7.
When the empty area for two sectors is formed, intermittent reproduction is resumed promptly, and the decoding data for two sectors are made to memorize.
As a result, even if the recording track of the portion reproduced accidentally is reproduced again and it makes right decoding data memorize, reading memorized decoding data [memory / 7 / in a this third-time raw period], when a reproduction error occurs by track jump etc. can be continued.
[0007]Data decompression of the decoding data inputted into the ATRAC decoder 8 one by one is carried out per sound group, and they are inputted into DA conversion circuit 9. As a result, it is drawn from said DA conversion circuit 9, without a reproduced sound signal breaking off. The composition of drawing 2 is a circuit block figure extracting and showing reproduction portions according to the description of the recorder of page [160th] drawing 1 of a report mentioned above.
[0008]
[Problem(s) to be Solved by the Invention]However, in the conventional composition mentioned above, if it reads one by one, always storing a lot of data by memorizing the constant rate of decoding data in a memory at the time of fast reproduction, it will compare between the speech information memorized and the speech information read at the time of ordinary reproduction, and a lengthy time delay will be produced. Therefore, even if a user checks a playback voice and cancels fast forwarding reproduction to the optimal timing, ** et al., the pickup has countered the

position which passed the position corresponding to the optimal timing substantially, and it becomes difficult to search reproduce [which is expected also as ordinary reproduction as it is] it.
[0009]Then, it is necessary to abolish most time delay for the reproduced sound signal at the time of fast reproduction.
[0010]
[Means for Solving the Problem]Then, this invention provides a storage-unit setting circuit which specifies reproduction compression audio data volume which carries out a selective memory so that memorized data in said memory may be mostly read by the next memory start during high speed reproduction mode set time.
[0011]
[Function]Therefore, according to this invention, the data in which only the minimum was accumulated in the memory but data was memorized is mostly read by the start of the following selective memory.
[0012]
[Example]Hereafter, this invention is explained according to working example illustrated to drawing 1. The composition illustrated to the memory controller 6 and the system controller 10 so that this invention may be adopted as the minidisc player illustrated also to drawing 2 and it may illustrate to ** Li and drawing 1 is used for this example.
[0013]In the player of this example, setting out of high speed reproduction mode is interlocked with, and the mode setting means 100 of the system controller 10 supplies a reset pulse to the memory address generating means 64 and the read address generating means 66, A memory address and a read address are set as an initial value by setting out of high speed reproduction mode. The memory controller 6 which inputs decoding data detected the header added to the head part of each sector in decoding data in the state of the continuous scan of the optical pickup 1 in the header detection circuits 60, and has inputted the detected header into the sector detector circuit 61. A header comprises the number of a cluster and the number of a sector which are the units of intermittent recording, ** also detects only the sector in which speech information is included with the even number sector to which a sound group does not become discontinuous, and said sector detector circuit 61 supplies a data storage timing output to the storage-unit setting circuit 62. This storage-unit setting circuit 62 presets the designated value which the storage-unit setting means 104 in a system controller generates, and supplies a storing command to the memory address generation circuit 63 only within the sound group period corresponding to a designated value synchronizing with a data storage timing output. As a result, the decoding data equivalent to specification sound group number are memorized by said memory 7.
[0014]Said storage-unit setting circuit 62 supplies the jump instructions generated synchronizing with de-energizing of a storing command to the track jump commanding means 103, and this track jump commanding means 103 supplies a fixed number of jump pulses to the servo circuit 13, and it performs the track jump of a fixed count. After the end of this track jump, if said pickup 1 starts a reproducing scan stably, decoding data will be supplied to the header detection circuits 60, and will repeat the fast reproduction mentioned above.
[0015]In this example, it may be divided and recorded on the area which the program currently recorded on the disk was not always continuously recorded on single area, and was left on the way. However, when division recording is carried out to the area which the same program left, the always end address of each division area which constitutes a common program is recorded on the user TOC area located in the start portion of record TORATSU.

[0016]Then, the system controller 10 has memorized the TOC data reproduced by a reproduction initial state in the TOC memory 101, When the program searching means 102 compares the address information and TOC data into which during the period of fast reproduction is inputted from the EFM decoder 4 and fast reproduction reaches near the termination of division area, Access instructions are supplied to the track jump commanding means 103 so that the start edge of the division area which said optical pickup 1 should reproduce next may be accessed.
[0017]As a result, the track jump commanding means 103 generates a track jump pulse continuously according to migration length, and carries out high speed movement of the playback position of said optical pickup 1 at a stretch to the start edge of the next division area. Although the TOC memory 101 was formed in the system controller in drawing 1, it is better to use a part of memory 7, when there is much TOC information, and there is no special meaning which provides a TOC memory in a system controller.
[0018]On the other hand, it has generated the read address in order to read decoding data per sound group from said memory 7, whenever the read address generation circuit 65 is inputted [the reading command of the ATRAC decoder 8]. as a result, decoding data are read at the rate of about 1 law. In this example, the designated value is set up according to the memory cycle of decoding data, and the designated value is set up with the sound group number of 1-8 according to the access characteristic of a player. This designated value is set as the sound group number of the grade from which the memorized decoding data are mostly read by the next memory start, and it is preset by said storage-unit setting means 104.
It is a value set up for every player with the characteristic of said optical pickup 1, the number of track jumps per time at the time of fast reproduction, etc.

[0019]As a result, like [the case where the optical pickup 1 moves between division area, and when the reproduction timing of the sector memorized after a track jump is overdue], when the timing of a memory start is late for a schedule, the data which should be read runs short. When the data read from said memory 7 runs short, the ATRAC decoder 8 generates a noise. So, in this example, lack of stored data is detected in the storage capacity detector circuit 64, and the lack detect output is supplied to the ATRAC decoder 8. Said ATRAC decoder 8 is constituted so that mute of the output may be carried out at the time of a lack detect output input. Therefore, a noise does not occur from said ATRAC decoder 8 at the time of missing of data.
[0020]The system controller 10 in a figure comprises software of the microcomputer.
Although the memory controller 6 comprises hardware, it is not necessary to necessarily carry out clear distinction to the appearance in this invention.
Drawing 3 is an explanatory view showing the relation of a tracking error output with memory address change of this example, and read address change typically.
[0021]After performing renewal of an address for [of a designated value] a sound group, a memory address interrupts updating after sector detection, so that more clearly than drawing 3. A reproduction address updates a read address per sound group periodically. As a result, in this example, according to read-out instructions of an ATRAC decoder, 1 sound group ** [every] decoding data are read, and most decoding data beforehand memorized by the next memory start are altogether read so that more clearly than change of the reading address shown with a dashed dotted line. Therefore, when the start of memory is overdue, a silent period is formed just before memory, and mute mentioned above is performed. Also when drawn without decoding data forming a window period, speech information becomes discontinuous by the discontinuous part used as the joint of intermittent memory, and a noise will be generated. Then, it cannot be

overemphasized that it may constitute so that the read-out pause for 1 sound group may be performed and mute may be carried out [sound / in the period] near a break point if needed.
[0022]Said optical pickup 1 will memorize the decoding data for a specification sound group period after sector detection, will perform the track jump for prescribed frequency according to the jump instructions generated immediately after memory, will be in a continuous reproduction scanning state after a jump, and searches a sector. Said optical pickup 1 repeats the operation mentioned above, and performs fast reproduction.
[0023]
[Effect of the Invention]Therefore, according to this invention, even if voice data may break off at the time of fast reproduction, it is not behind, and positive access is attained, and the effect is size.

TECHNICAL FIELD

[Industrial Application]This invention relates to the fast reproduction circuit of a minidisc player.

PRIOR ART

[Description of the Prior Art]It is attached to the MD recorder which made audio record reproduction possible, and the 160-168th page of the December 9, 1991 item of the magazine "Nikkei electronics" of the Nikkei McGraw-Hill, Inc. issue succeeds in description. This MD recorder carries out the data compression of about 1/of the sounds for two channels to 5, carries out [sound / for about 2 seconds] intermittent recording as information for about 0.5 second, and forms a recording track, A sound is reproduced by memorizing in a memory and carrying out elongation processing of the read data for the memorized information to it continuously, reproducing this recording track one by one at the time of reproduction. The data configuration of one cluster of each intermittent recording track, The whole comprises 36 sectors and compression audio data is arranged as main data by 32 sectors in which indicative datas, such as words of karaoke, follow one sector which the fixed data no information is [fixed data] in three sectors to precede follow as link data as sub data.
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[Problem(s) to be Solved by the Invention]However, in the conventional composition mentioned above, if it reads one by one, always storing a lot of data by memorizing the constant rate of decoding data in a memory at the time of fast reproduction, it will compare between the speech information memorized and the speech information read at the time of ordinary reproduction, and a lengthy time delay will be produced. Therefore, even if a user checks a playback voice and cancels fast forwarding reproduction to the optimal timing, ** et al., the pickup has countered the position which passed the position corresponding to the optimal timing substantially, and it

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MEANS

[Means for Solving the Problem]Then, this invention provides a storage-unit setting circuit which specifies reproduction compression audio data volume which carries out a selective memory so that memorized data in said memory may be mostly read by the next memory start during high speed reproduction mode set time.

OPERATION

[Function]Therefore, according to this invention, the data in which only the minimum was accumulated in the memory but data was memorized is mostly read by the start of the following selective memory.

EXAMPLE

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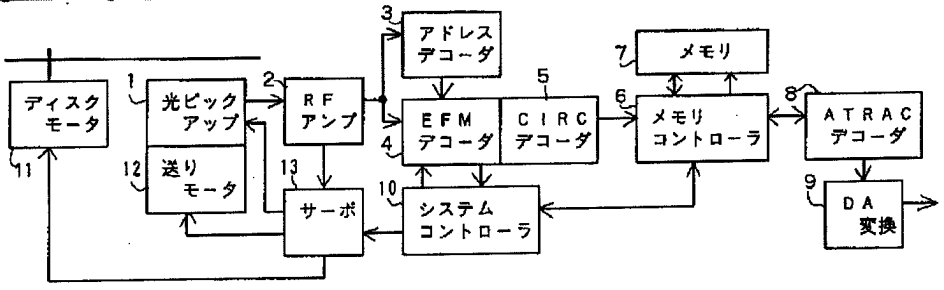
DESCRIPTION OF DRAWINGS

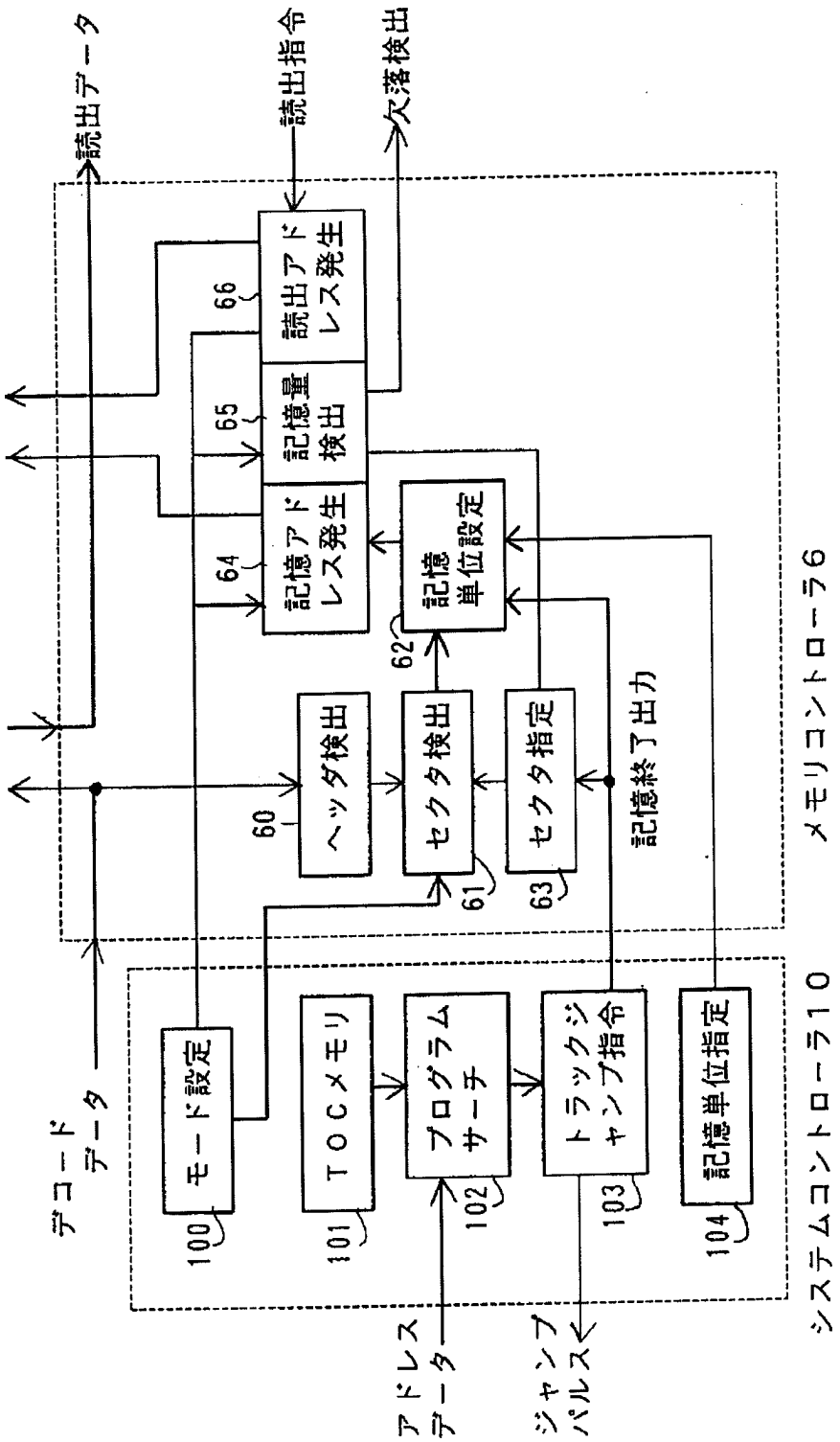
[Brief Description of the Drawings]
[Drawing 1]It is a detailed circuit block figure of the memory controller which adopts this invention.
[Drawing 2]It is a regenerative-circuit block diagram of a minidisc player.
[Drawing 3]It is an explanatory view showing change of a memory address and a reproduction address.
[Description of Notations]
7 Memory
62 Storage-unit setting circuit

DRAWINGS

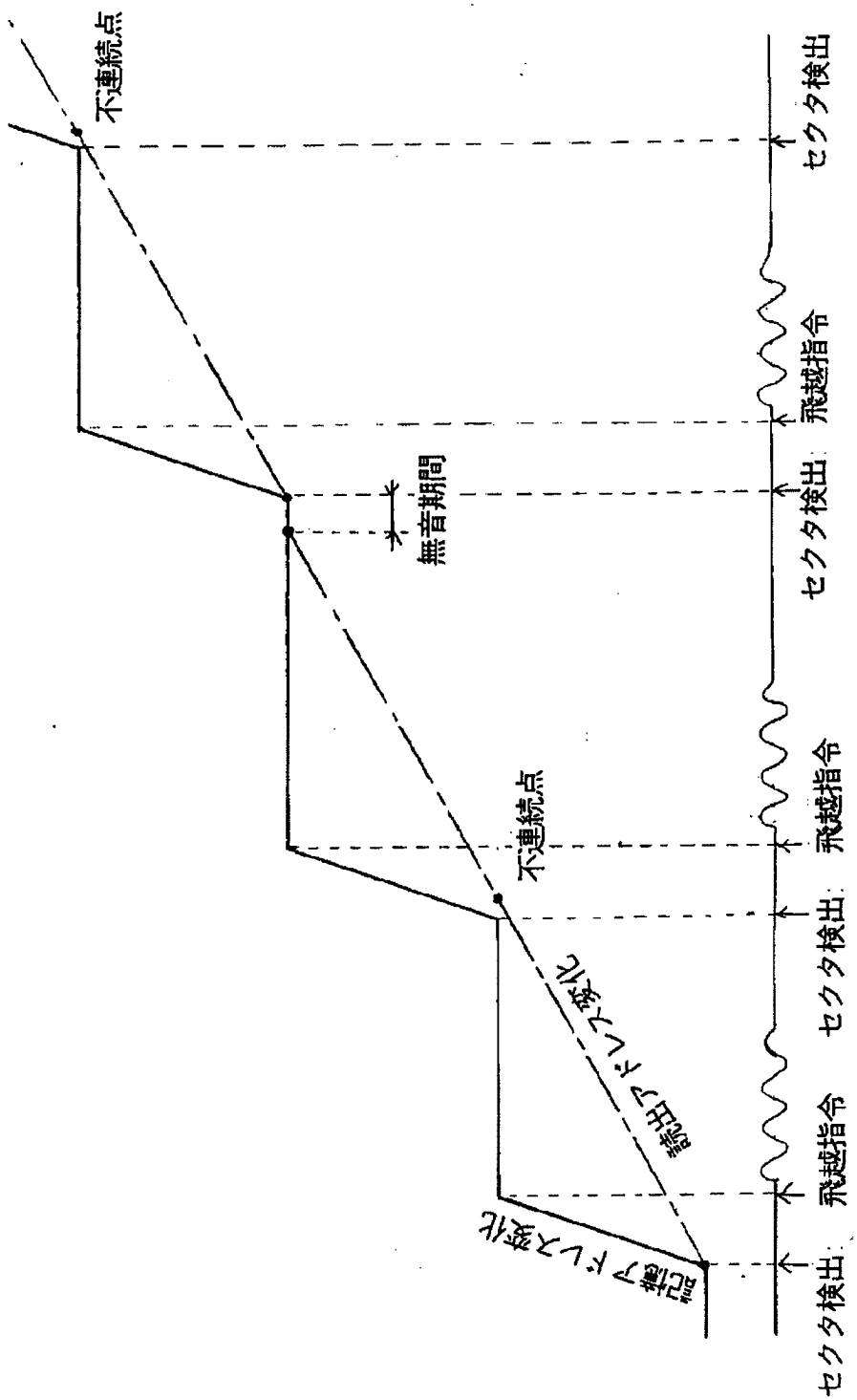
[Drawing 2]



[Drawing 1]


読出データ
読出指令
欠落検出
読出アドレス発生
66
記憶量検出
65
記憶アドレス発生
64
記憶単位設定
62
ヘッダ検出
60
セクタ検出
61
セクタ指定
63
記憶終了出力
メモリコントローラ6
デコードデータ
モード設定
100
TOCメモリ
101
プログラムサーチ
102
トラックジャンプ指令
103
記憶単位指定
104
システムコントローラ10
アドレスデータ
ジャンプパルス

[Drawing 3]


不連続点
無音期間
不連続点
セクタ検出
飛越指令
セクタ検出
飛越指令
セクタ検出
飛越指令
セクタ検出

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報（Ａ）**　(11)特許出願公開番号

特開平5－274798

(43)公開日　平成５年(1993)10月22日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｇ１１Ｂ　20/10	３２１　Ｚ	7923－5D		
7/00	Ｒ	9195－5D		
19/02	Ｄ	7525－5D		
27/10	Ａ	8224－5D		

審査請求　未請求　請求項の数１(全　６　頁)

(21)出願番号　特願平4－74110

(22)出願日　平成４年(1992)３月30日

(71)出願人　000001889
三洋電機株式会社
大阪府守口市京阪本通２丁目18番地
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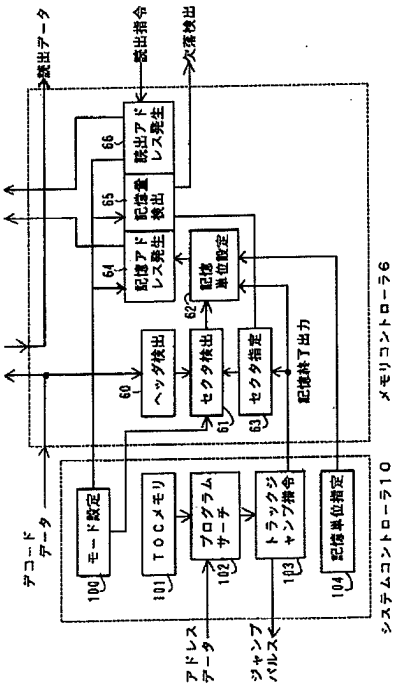
(74)代理人　弁理士　西野　卓嗣

(54)【発明の名称】　高速再生回路

(57)【要約】
【目的】　ミニディスクプレーヤで応答遅れのない高速再生を実現する。
【構成】予め連続再生記憶するサウンドグループ数を指定値として記憶単位指定手段１０４に設定しておき、高速再生モードの設定に際して指定値を記憶単位設定回路６２に記憶する。デコードデータをヘッダ検出回路６０を介してセクタ検出回路６１に入力し記憶タイミングを検出し、このタイミングに同期して記憶単位設定回路６２より指定値相当期間分の記憶指令を発生させ、記憶アドレス発生回路６４より記憶アドレスを発生して所定サウンドグループ数分のデコードデータをメモリに記憶させ、ＡＴＲＡＣデコーダより発せられる読出指令により読出アドレス発生回路６６より順次サウンドグループ単位でメモリよりデコードデータを読み出す。



【特許請求の範囲】
【請求項１】　データ圧縮した音声データを記録したスパイラル状記録トラックをトラックジャンプし乍ら間欠再生することにより得られる再生圧縮音声データを一定量選択してメモリに順次記憶し、前記メモリより順次読み出したデータをデータ伸長処理して高速再生音声信号を形成するミニディスクプレーヤに於て、
高速再生モード設定期間中に、前記メモリ内の記憶されたデータが次の記憶開始迄にほぼ読み出される様に、選択記憶する再生圧縮音声データ量を規定する記憶単位設定回路を、設けることを特徴とする高速再生回路。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、ミニディスクプレーヤの高速再生回路に関する。
【０００２】
【従来の技術】日経マグロウヒル社発行の雑誌「日経エレクトロニクス」の１９９１年１２月９日号の第１６０～１６８頁には、音声の記録再生を可能にしたミニディスクレコーダに付いて解説が為されている。このミニディスクレコーダは、２チャンネル分の音声を約１／５にデータ圧縮して約２秒分の音声を約０．５秒の情報として間欠記録して記録トラックを形成し、再生時にはこの記録トラックを順次再生しながらメモリに記憶し、記憶した情報を連続して読み出しデータを伸長処理することにより音声を再生するものである。各間欠記録トラックの１クラスタのデータ構成は、全体が３６セクタで構成され、先行する３セクタには情報のない固定データがリンクデータとして、続く１セクタにカラオケの歌詞等の表示データがサブデータとして、また更に続く３２セクタには圧縮音声データがメインデータとして配列されている。
【０００３】また、各セクタの先頭部分にはヘッダと称されるアドレスデータが設けられており、このアドレスデータには、クラスタ番号とセクタ番号が付加されている。従って、サブデータはこのセクタ番号を検出して識別できる。更に、２セクタのメインデータは、１１個のサウンドグループを含んでおり、再生はこの２セクタを単位に間欠再生が為される。その結果、通常再生時にはメモリに最大限の再生データが記憶されるように構成される。
【０００４】図２は、このミニディスクレコーダの再生部分の回路ブロック図である。ディスクの記録トラックを光学的に再生する光ピックアップ１は、その再生出力をＲＦアンプ２に入力して増幅した出力をサーボ回路１３とアドレスデコーダ３とＥＦＭデコーダ４に入力している。前記サーボ回路１３は、再生増幅出力よりトラッキング制御信号とフォーカス制御信号を形成し、前記光ピックアップ１と送りモータ１２に供給すると共に、システムコントローラ１０を介して得られる同期信号に基づいて形成される回転制御信号を形成してディスクモータ１１に供給している。従って、ディスクは前記ディスクモータ１１によって線速度一定に保たれ、前記ピックアップ１は、正しく記録トラックに追随すると共にその焦点を記録トラック面に一致させる。
【０００５】また、前記アドレスデコーダ３は、再生増幅出力の内トラッキングエラー信号の高域成分をＦＭ復調して得られるＡＤＩＰコードを検出してＥＦＭデコーダ４に入力している。該ＦＭデコーダ４は、前記システムコントローラ１０より得られる選択信号に従って、ＥＦＭデコーダ４内で検出されるサブコード又は、入力されるＡＤＩＰコードを選択して前記システムコントローラ１０に供給している。更に、前記ＥＦＭデコーダ４は、サブコードと共に同期信号をも分離しており、同期信号をシステムコントローラ１０に供給している。前記システムコントローラ１０は、同期信号をサーボ回路１３に供給すると共に、再生位置を示すサブコードまたはＡＤＩＰコードに基づきピックアップのアクセス制御を実行し、飛び越し走査による間欠再生を可能にしている。
【０００６】ＥＦＭ復調されたデータは、ＣＩＲＣデコーダ５に於てエラー訂正等の処理を施されメモリコントローラ６に入力される。このメモリコントローラ６は、光ピックアップ１の飛び越し再生により繰り返し入力されるデコードデータを２セクタづつ更新記憶して前記メモリ７に記憶させると共に、後段のＡＴＲＡＣデコーダ８の読出指令に従って前記メモリ７に記憶されたデータをサウンドグループ単位で順次読み出している。更に、前記メモリコントローラ６は、メモリ７に対して常に最大限のデコードデータを記憶させており、２セクタ分の空きエリアが形成されたときには直ちに間欠再生を再開し、２セクタ分のデコードデータを記憶させる。その結果、トラック飛び等により再生エラーが発生した場合には、誤って再生された部分の記録トラックを再度再生して正しいデコードデータを記憶させても、この再再生期間中メモリ７より記憶済みのデコードデータを読み出し続けることが出来る。
【０００７】ＡＴＲＡＣデコーダ８に順次入力されるデコードデータは、サウンドグループ単位でデータ伸長されＤＡ変換回路９に入力される。その結果、前記ＤＡ変換回路９からは、再生音声信号が途切れることなく導出される。尚、図２の構成は、前述する記事の第１６０頁の図１のレコーダの記載に準じて再生部分を抽出して示す回路ブロック図である。
【０００８】
【発明が解決しようとする課題】しかし、上述する従来の構成に於て、高速再生時にデコードデータの一定量をメモリに記憶することにより常時多量のデータを蓄積しながら順次読み出すと、記憶される音声情報と読出される音声情報との間に通常再生時に比し大幅な時間的遅れ

を生ずる。従って、使用者が再生音声を確認し乍ら最適のタイミングで早送り再生を解除しても、ピックアップはその最適タイミングに対応する位置を大幅に通過した位置に対向しており、そのまま通常再生としても期待する頭出し再生が困難となる。

【０００９】そこで、高速再生時の再生音声信号を時間的な遅れを殆どなくす必要がある。

【００１０】

【課題を解決するための手段】そこで、本発明は、高速再生モード設定期間中に、前記メモリ内の記憶されたデータが次の記憶開始迄にほぼ読み出される様に、選択記憶する再生圧縮音声データ量を規定する記憶単位設定回路を、設けることを特徴とする。

【００１１】

【作用】よって、本発明によれば、データは最小限しかメモリに蓄積されず、記憶されたデータは次の選択記憶の開始迄にほぼ読み出される。

【００１２】

【実施例】以下、本発明を図１に図示する実施例に従い説明する。本実施例は、図２にも図示するミニディスクプレーヤに本発明を採用するものであり、図１に図示する様にメモリコントローラ６とシステムコントローラ１０に図示する構成を採用することを特徴とする。

【００１３】本実施例のプレーヤでは、高速再生モードの設定に連動してシステムコントローラ１０のモード設定手段１００が記憶アドレス発生手段６４と読出アドレス発生手段６６にリセットパルスを供給し、高速再生モードの設定により記憶アドレスと読出アドレスを初期値に設定する。デコードデータを入力するメモリコントローラ６は、光ピックアップ１の連続走査状態でヘッダ検出回路６０にてデコードデータ中の各セクタの先頭部分に付加されたヘッダを検出し、検出したヘッダをセクタ検出回路６１に入力している。ヘッダは、間欠記録の単位であるクラスタの番号とセクタの番号より成り、前記セクタ検出回路６１は、サウンドグループが不連続にならない偶数セクタで然も音声情報が含まれているセクタのみを検出してデータ記憶タイミング出力を記憶単位設定回路６２に供給する。この記憶単位設定回路６２は、システムコントローラ内の記憶単位指定手段１０４が発生する指定値をプリセットし、データ記憶タイミング出力に同期して指定値に対応するサウンドグループ期間に限って記憶指令を記憶アドレス発生回路６３に供給する。その結果、前記メモリ７には指定サウンドグループ数に相当するデコードデータが記憶される。

【００１４】前記記憶単位設定回路６２は記憶指令の消勢に同期して発生される飛び越し指令をトラックジャンプ指令手段１０３に供給しており、このトラックジャンプ指令手段１０３は一定数のジャンプパルスをサーボ回路１３に供給し、一定回数のトラックジャンプを実行させる。このトラックジャンプの終了後、前記ピックアップ１が安定に再生走査を開始すると、デコードデータがヘッダ検出回路６０に供給され、上述する高速再生を繰り返す。

【００１５】本実施例では、ディスクに記録されているプログラムが単一エリアに連続的に記録されているとは限らず、途中で離れたエリアに分割されて記録されていることもある。しかし、同一プログラムが離れたエリアに分割記録されている場合には、記録トラッの開始部分に位置するユーザＴＯＣエリアに、共通プログラムを構成する各分割エリアの始終端アドレスが記録されている。

【００１６】そこで、システムコントローラ１０は再生初期状態で再生されるＴＯＣデータをＴＯＣメモリ１０１に記憶しており、プログラムサーチ手段１０２は高速再生の期間中もＥＦＭデコーダ４より入力されるアドレスデータとＴＯＣデータを比較して高速再生が分割エリアの終端近傍に達したとき、前記光ピックアップ１が次に再生すべき分割エリアの始端をアクセスする様にアクセス指令をトラックジャンプ指令手段１０３に供給する。

【００１７】その結果トラックジャンプ指令手段１０３は、トラックジャンプパルスを移動距離に応じて連続的に発生し、前記光ピックアップ１の再生位置を一気に次の分割エリアの始端まで高速移動させる。尚、図１中ではシステムコントローラ内にＴＯＣメモリ１０１を設けたが、ＴＯＣ情報が多い場合にはメモリ７の一部を利用した方が良く、システムコントローラ内にＴＯＣメモリを設ける特別の意味はない。

【００１８】一方、読出アドレス発生回路６５は、ＡＴＲＡＣデコーダ８の読出指令が入力される度に前記メモリ７よりサウンドグループ単位でデコードデータを読み出すべく読出アドレスを発生している。その結果、デコードデータはほぼ一定の速度で読み出される。本実施例では、デコードデータの記憶周期に合わせて指定値を設定しており、その指定値は、プレーヤのアクセス特性に応じて１～８のサウンドグループ数で設定される。この指定値は、記憶したデコードデータが次の記憶開始迄にほぼ読み出される程度のサウンドグループ数に設定され、前記記憶単位指定手段１０４にプリセットされており、前記光ピックアップ１の特性や、高速再生時の１回当りのトラックジャンプ数等によってプレーヤ毎に設定される値である。

【００１９】その結果、光ピックアップ１が分割エリア間で移動する場合や、トラックジャンプ後に記憶するセクタの再生タイミングが遅れた場合の様に、記憶開始のタイミングが予定より遅れた時には、読み出すべきデータが不足する。前記メモリ７より読み出すデータが不足する場合は、ＡＴＲＡＣデコーダ８がノイズを発生する。そこで本実施例では、記憶量検出回路６４で記憶データの欠落を検出し、欠落検出出力をＡＴＲＡＣデコー

ダ8に供給している。前記ＡＴＲＡＣデコーダ8は、欠落検出出力入力時に出力をミュートする様構成されている。よって、データ欠落時に前記ＡＴＲＡＣデコーダ8よりノイズが発生することはない。

【００２０】尚、図中のシステムコントローラ１０は、マイクロコンピュータのソフトウエアで構成されており、メモリコントローラ6はハードウエアで構成されているが、本発明では、必ずしもその様に明確な区別をする必要はない。図3は、本実施例の記憶アドレス変化と、読出アドレス変化と、トラッキングエラー出力の関係を模式的に示す説明図である。

【００２１】図3より明らかな様に、セクタ検出後、記憶アドレスは指定値相当のサウンドグループ分のアドレス更新を実行した後、更新を中断する。再生アドレスは、定期的にサウンドグループ単位で読出アドレスを更新する。その結果、一点鎖線で示す読み出しアドレスの変化より明らかな様に、本実施例ではＡＴＲＡＣデコーダの読み出し指令に従って１サウンドグループずづつデコードデータが読み出され、次の記憶開始迄に予め記憶されていたデコードデータを殆ど全て読み出す。従って、記憶の開始が遅れた場合は記憶の直前に無音期間が形成され、前述するミュートが実行される。尚、デコードデータが空白期間を形成することなく導出される場合にも、間欠記憶の継ぎ目となる不連続部分で音声情報が不連続となりノイズを発生することになる。そこで必要に応じて不連続点付近で１サウンドグループ分の読出休止を実行しその期間中音声をミュートする様に構成しても良いことは言うまでもない。

【００２２】更に、前記光ピックアップ１はセクタ検出後、指定サウンドグループ期間分のデコードデータを記憶し、記憶直後に発生される飛越指令に従って所定回数分のトラックジャンプを実行し、ジャンプ後に連続再生走査状態となってセクタを検索する。前記光ピックアップ１は、上述する動作を繰り返し高速再生を実行する。

【００２３】

【発明の効果】よって、本発明によれば、高速再生時に音声データが途切れることはあっても遅れることはなく、確実なアクセスが可能となりその効果は大である。

【図面の簡単な説明】

【図１】本発明を採用するメモリコントローラの詳細回路ブロック図である。

【図２】ミニディスクプレーヤの再生回路ブロック図である。

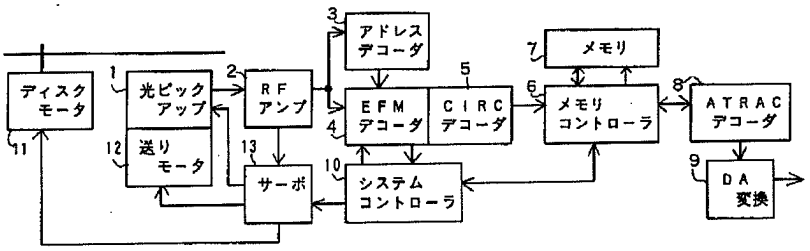
【図３】記憶アドレスと再生アドレスの変化を示す説明図である。

【符号の説明】

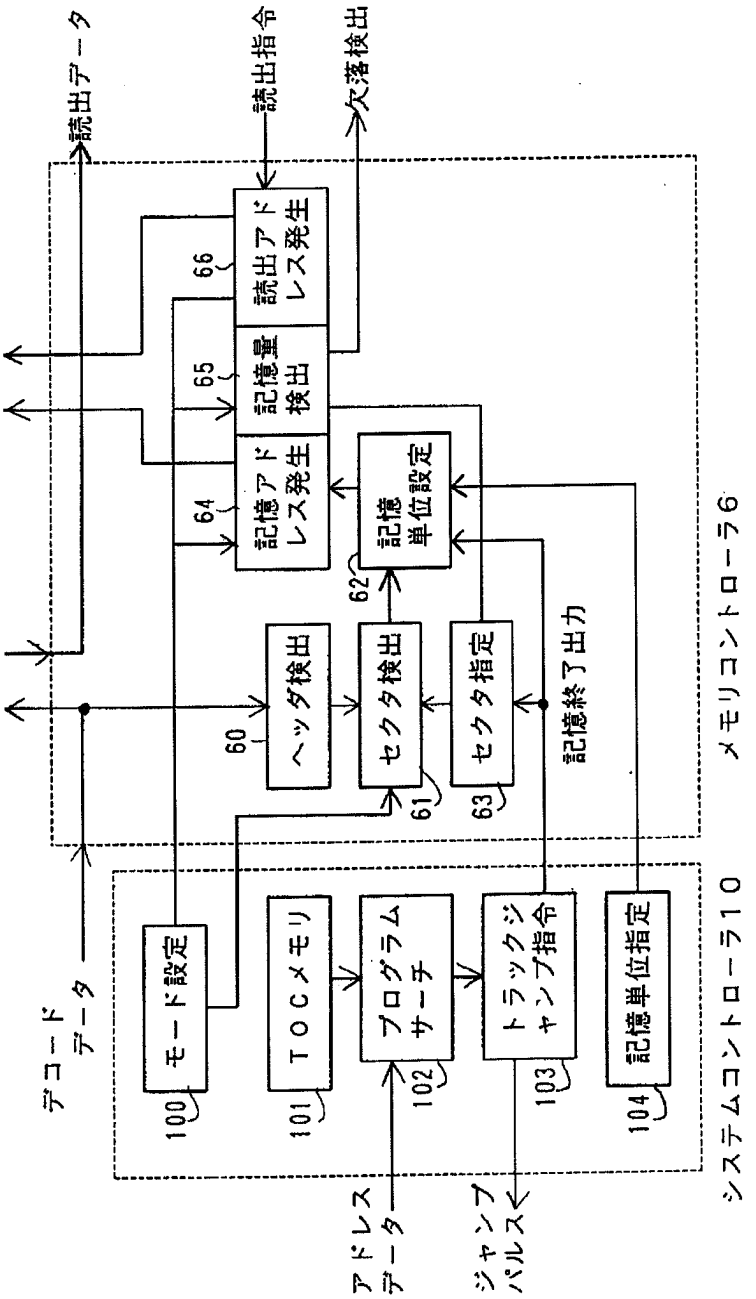
７　メモリ

６２　記憶単位設定回路

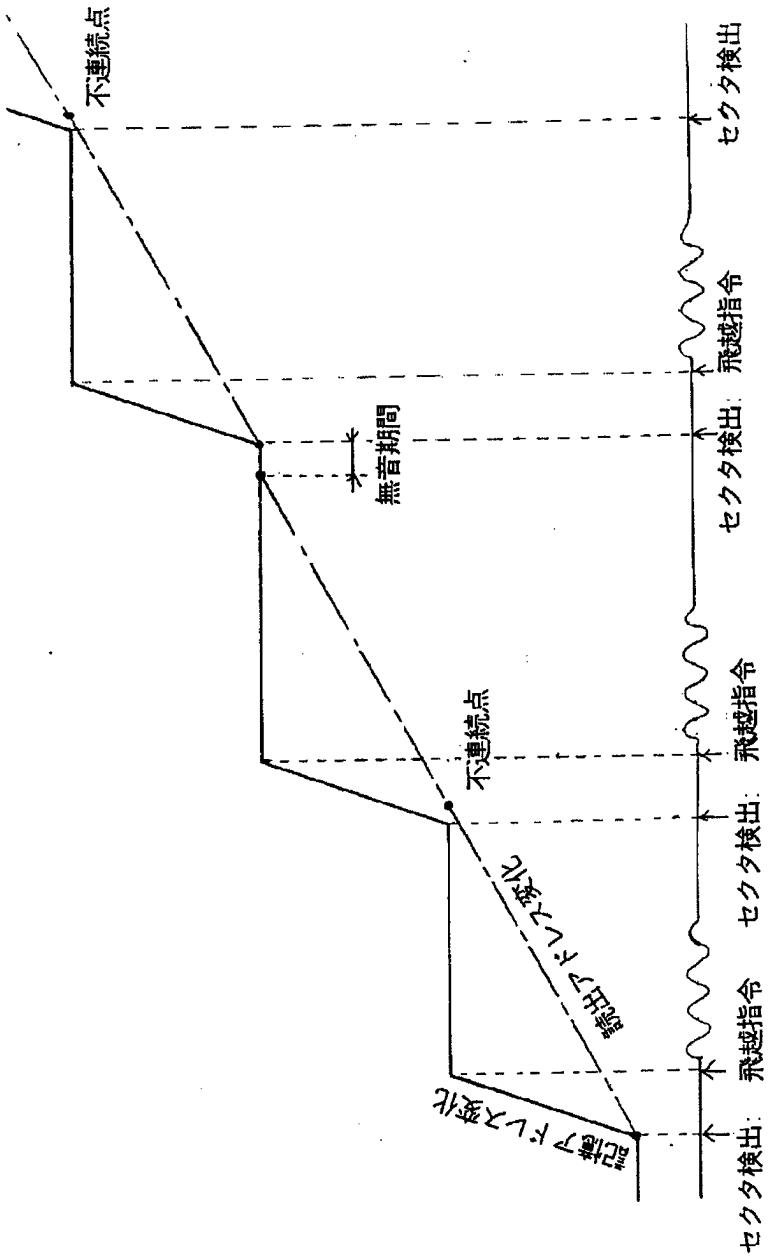
【図２】



【図1】


読出データ
読出指令
欠落検出
読出アドレス発生
記憶量検出
記憶アドレス発生
記憶単位設定
ヘッダ検出
セクタ検出
セクタ指定
記憶終了出力
メモリコントローラ6
モード設定
TOCメモリ
プログラムサーチ
トラックジャンプ指令
記憶単位指定
システムコントローラ10
デコードデータ
アドレスデータ
ジャンプパルス
60
61
62
63
64
65
66
100
101
102
103
104

【図3】


不連続点
無音期間
不連続点
記録データレス変化
セクタ検出
飛越指令
セクタ検出
飛越指令
セクタ検出
飛越指令
セクタ検出